

Design and Implementation of Digital Beam Former Architecture for Phased Array Radar

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Abstract—This paper deals with the design and implementation of a digital beam former architecture which is developed for 4/8/12/16 element phased array radar. This technique employs a very high performance FPGA to handle large no of parallel complex arithmetic operations including digital down conversion and filtering. A 3MHz echo signal riding on an IF carrier of 60 MHz is under sampled at 50 MHz and down converted digitally to bring the spectrum to echo signal baseband. After suitable decimation filtering, the I and Q channels are multiplied with Recursive Least Squares based optimized complex weights to form partial beams. The prototype architecture employs techniques of pipelining and parallelism to generate multiple beams simultaneously from a 16 element array within 1 μ sec. This can be extended to several number of arrays. The critical components employed in this design are eight 16 bit 125 MS/s ADCs and a very high performance state of the art Xilinx FPGA device Virtex-5 FX 130T having several on-chip resources and 150 MHz clock generators.

Keywords— RLS, DBF, FPGA, DDC, ADC, ASIC.

I. INTRODUCTION

Recent trends in VLSI [2] technology have made it possible for the designers to transform several complex DSP algorithms into efficient architectures that fit into very small high performance Application Specific Integrated Circuits (ASICs)[5] or Field Programmable Gate Array (FPGA) devices such as Virtex-5 or Stratix-3. The Digital Beam Forming (DBF) is a marriage between the antenna technology and digital technology. The digital methods for antenna beam forming in the receiving mode of radar can be advantageous in providing the system with high degree of flexibility in “Beam-Pattern Management”.

In conventional beam former the measurement of a propagating, coherent wave front, relative to ambient background noise and spatially localized interferences is enhanced by coherent processing of data collected with an array of sensors. This is achieved by time delaying and summing weighted sensor data. In receive mode, beam formers output the weighted sum of the sensor signals, reducing the signal dimensions from the number of elements to one. DBF, which can be employed at both receive and transmit ends has the inherent advantages of adaptive nulling, high gain, low side lobe levels, closely placed multiple beam, flexible radar power and time management.

DBF is based on the conversion of the RF signal at each Antenna Elements into two streams of binary base band

signals representing I and Q channels. These two digital base band signals can be used to recover both the amplitudes and phases of the signals received at each element of the array. The availability of faster multi-byte A/D converters enable the received data through antenna to be sampled at Nyquist sampling rate and processed in digital domain. With ever increasing processing speed and computation power, the computation of multiple beams can be performed digitally using VLSI[5] rather than in RF. Hence the number of simultaneous beams only depends on the speed of A/D conversion and its resolution (number of bits), processor speed and its processing capacity. The process of digital beam forming implies weighting the input samples by a complex weighting function and then adding together to form the desired output. The end product of this processing is a set of beams differently oriented in space, each beam giving access to a number of range and Doppler cells [10].

The key tasks involved in the DBF are:

- Accurate translation of the analog signal into the digital regime using high speed ADCs in parallel,
- Digital Signal Processing of these high speed samples for the tasks like digital mixing, down converting digital filtering and performing complex arithmetic operations.
- Providing high speed data communication for receiving weights and sending beams for further processing and plotting.

II. MODELING AND DATA FLOW OF DBF

The following flow chart in Fig.1 explains the Digital Beam Forming which has been designed, simulated and implemented on the hardware. It shows the data flow for beam formation for sixteen Transmit/ Receive (T/R) elements. During the receive mode of radar operation, the echo received is amplified and filtered using band pass filter [8] to obtain RF. The IF stage converts RF into IF using one or two stages of Local Oscillator (LO) mixing and filtering. The IF, generally in the range of tens of MHz, is digitized using high speed ADC and sampling clock. The criteria to select this sampling clock is as per the Nyquist rate i.e, the sampling clock should be greater or equal to twice the bandwidth of the IF signal, however in our design, we sub-sample the input

signal exploiting the band pass sampling technique to avoid digitizing the full band unnecessarily.

The digital IF signal is then disassembled into In-phase (I) and Quadrature phase signal (Q). Further the sixteen elements are divided into four sub arrays each consisting of four elements. Sub-arraying is done to reduce the design complexity. During each dwell, the radar computer sends some beam parameters to calculate the required weights. This design considers fixed weights to prove the DBF concept

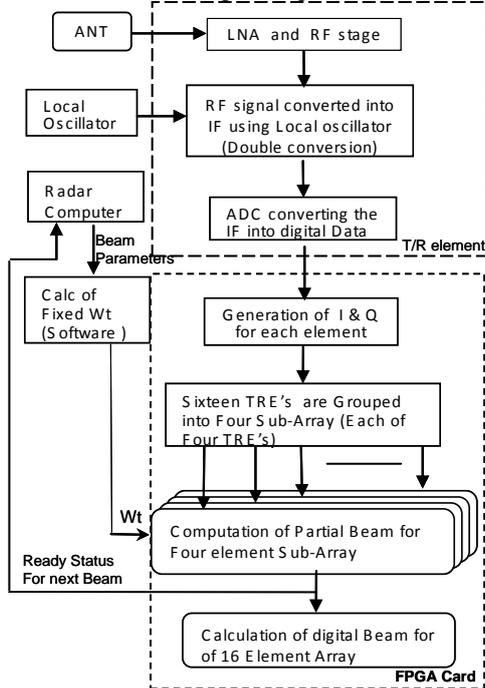


Fig.1 Multiple Digital Beam Former Data Flow

Partial beam for the sub array is computed by the complex multiplications of I & Q data and the fixed weights, which is calculated for each dwell in the software. Thus, the summation of the partial beams of all the four sub arrays yields the final beam for sixteen element array. These results are sent to signal processor for further processing.

III. BEAM FORMING METHODS

For beam forming, the complex baseband signal $S(t)$ (eq 3.1) is multiplied by the complex weight vector W_k (eq 3.2) considering the phase shift and amplitude scaling required for each antenna element. Eq 3.3 will give the Digital Beam in the direction of the corresponding weight used with usual notation.

$$S(t) = x(t) + j y(t) \quad \dots\dots 3.1$$

$$W_k = A_k e^{j\theta_k} = A_k \cos(\theta_k) + j A_k \sin(\theta_k) \quad \dots\dots 3.2$$

Where

W_k is complex weight for the K th antenna element, A_k is the relative amplitude of the weight and θ_k is the phase shift of the weight.

Virtex-V FPGA can implement the complex multiplication of weights and baseband signal $S(t)$ as shown below:

$$S_k(t) * W_k = A_k \{ [x_k(t) \cos(\theta_k) - y_k(t) \sin(\theta_k)] + j [x_k(t) \sin(\theta_k) + y_k(t) \cos(\theta_k)] \} \dots\dots\dots 3.3$$

To calculate the weights to form multiple receive beams. There are many algorithms like LMS, RLS and QR RLS[4] and so on. For the proposed architecture the weights are calculated using the RLS algorithm. For each one of the beams to be formed one set of weights needs to be calculated and stored in the memory.

A brief procedure to calculate the optimal weights using RLS algorithm is given below:

- i. Accept new samples $x(k)$ and the reference desired samples from the central element $d(k)$
- ii. Form $X(k)$ by shifting $x(k)$ into the information vector.
- iii. Compute the a priori output $y_0(k) = W_k^{oT} X(k)$
- iv. Compute the priori error, $e_0(k) = d(k) - y_0(k)$
- v. Compute the filtered information vector Z_k :

$$Z_k = R_k^{-1} X(k)$$

- vi. Compute the normalized error power q :
 $q = X^T(k) Z_k$
- vii. Compute the gain constant, $v = \frac{1}{1+q}$

- viii. Compute the normalized filtered information vector \hat{Z}_k :
 $\hat{Z}_k = v * Z_k$

- ix. Update the optimal weight vector W_k^0 to W_{k+1}^0 :
 $W_{k+1}^0 = W_k^0 + e_0(k) \hat{Z}_k$

- x. Update the inverse correlation matrix R_k^{-1} to R_{k+1}^{-1} in preparation for the next iteration :

$$R_{k+1}^{-1} = R_k^{-1} - \hat{Z}_k Z_k^T(k)$$

The reasons for exploring and using the RLS technique for calculation of the optimal weights are RLS can be numerically better behaved than the direct inversion of autocorrelation matrix and it provides an optional weight vector estimate at every sample time, while the direct methods compute the estimate only at the end of the data sequence.

IV. REALIZATION OF FIXED DBF

The Block diagram shown in Fig. 2 explains the architectural features of the DBF for Four element Phased Array antenna. This Architecture has been extended to 16 element array in this work and the same can be extended to any number of antenna arrays. The basic building blocks for this development are Digital Down Converters (DDC), complex adders and complex multipliers. The IF signal, generally in the range of 50 MHz to 60 MHz is converted into one word digital data using 8/16 bit, 125 MS/s high speed ADCs. The digital data is received at a sampling clock of 50 MHz and then processed as follows: 16 bit high speed ADC Data is passed through a digital Mixer consisting of a 50 MHz Numerically Controlled Oscillator (NCO), a multiplier (16x16 bit), suitable low pass decimation and compensating filters (CIC and CFIR filters) of bandwidth 5

MHz to filter the entire unwanted signal outside the band and a 10 rate decimator to bring down the sampling rate to 5 MS/s for further processing. Finally the DDC output will be In phase (I) and Quadrature (Q) signals. Fig. 3 gives the architectural details.

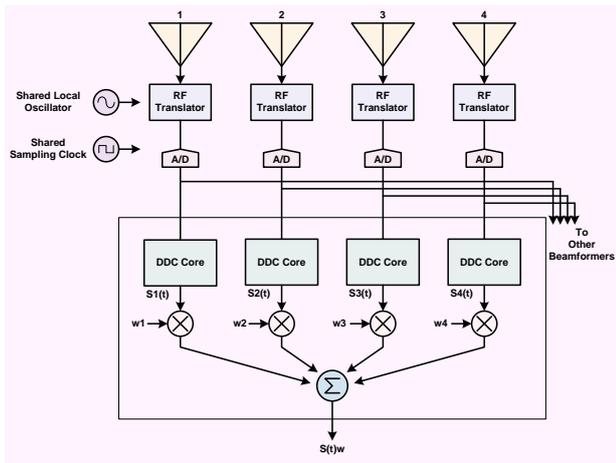


Fig 2. Four element DBF for multiple digital beams.

The 16-bit digital data is fed into FPGA from the 16 bit ADC for the generation of In -phase and Quadrature phase signals as explained above. The function of the I and Q generator is to multiply the incoming signal by the locally generated sinusoid to shift the spectrum of the signal.



Fig. 3 FPGA Based Digital Down Converter

A straightforward implementation uses two multipliers, one each for the sine and the cosine as shown in Fig. 4.

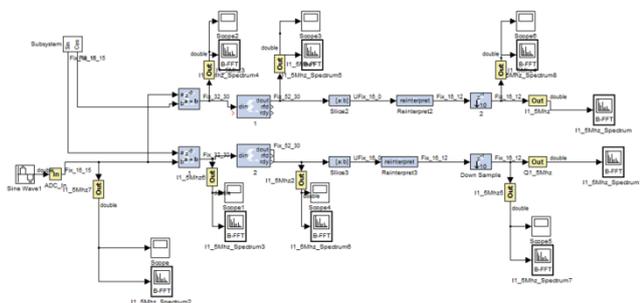


Fig. 4 Implementation of Digital Down Converter

By multiplying the input data, by the Quadrature sine and cosine waveforms, we achieve a frequency translation to the base band as shown in Fig. 5 below:

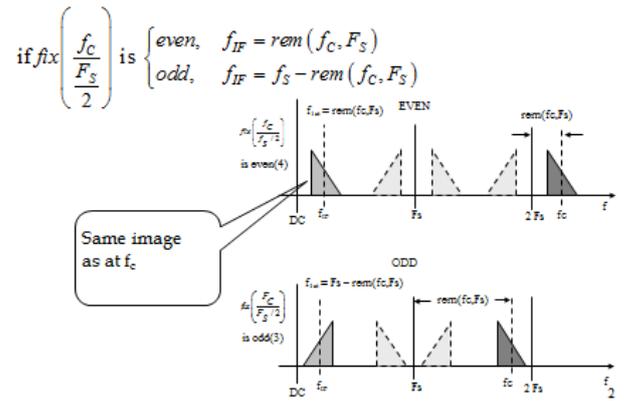


Fig. 5 Nyquist Zones for $f_c = 60$ MHz and $f_s = 50$ MHz

It can easily be seen that the base band signal will be positioned at 0 frequencies after decimation by 10 using the above formulae as well as the Nyquist zones shown.

The multipliers are 16 x 16 bit signed multipliers. The lower 16-bits, of the 32-bit output, are truncated and the 16 most significant bits are used for subsequent processing. The quantization error is within 0.1% and is acceptable. For realizing the 16 element array it is essential to have 16 different DDC modules in the complete architecture. Details are shown in the Fig 5. The complex multipliers and complex adders are implemented in hardware using VHDL. To perform this complex multiplication in FPGA we need to perform equivalent floating point arithmetic operations in fixed point as the error is within limits and this is faster when implemented in FPGA.

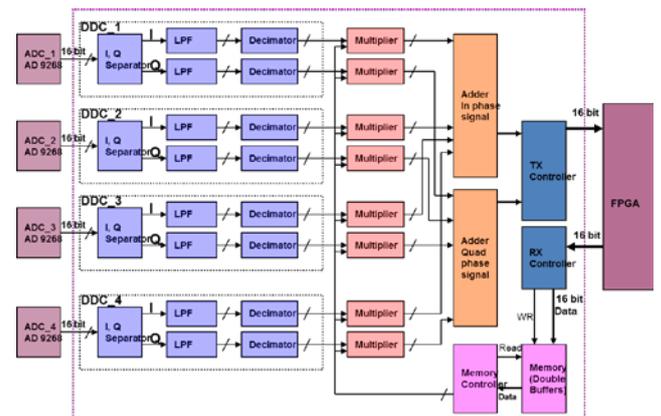


Fig.6 DBF Architecture for four element array.

The weights are calculated and stored in the memory of the FPGA. Depending upon the signal available from any direction within the range from -45 deg to +45 deg, suitable weights will be applied and the required number of beams will be calculated. During the formation of the beams it is assumed that direction of arrival is known apriori as the transmit beam is scheduled by the radar computer. With respect to the

direction of arrival, multiple beams are formed. The offset is fixed by the weights which are calculated and stored in the memory. With the developed architecture the weights are calculated for +/-10 deg, +/-20 deg and so on.

It is required to compute the complex multiplication for several numbers of weights which will decide where the beam needs to be formed. For sixteen elements to form one beam we need to have sixteen weights and for N number of beams, N different sets of sixteen weights are required. We consider the weights are fixed and calculated offline. The data flow architecture of the complex addition and complex multiplication are shown in Fig. 6 which is simulated using VHDL modeling and implemented on the prototype development hardware shown in Fig. 7. Summation of all the partial beams in the same digital domain, gives the full beam B(t), given by eq. 3.4 for an N-element Array.

$$B(t) = \sum_{k=0}^N S_k(t) * W_k \quad \dots\dots\dots 3.4$$

In case of multiple beams, the results are stored in FPGA / memory for processing.

Where,

- N : Number of T/R Elements
- W_k : Complex Weight of Kth Element
- S(t) : Received Signal

The Development Hardware used to implement this digital beam former architecture is shown in Fig.7 below:

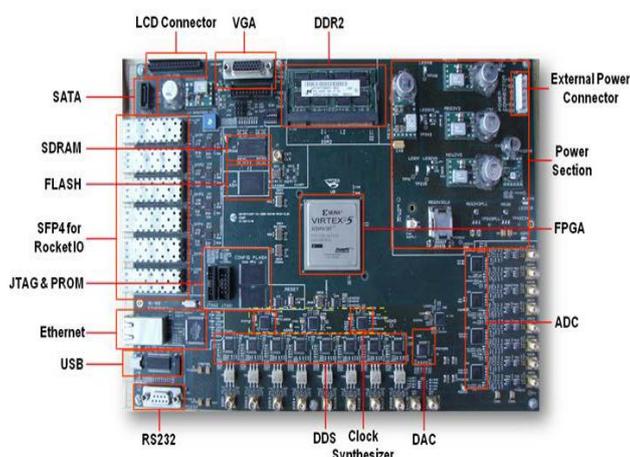


Fig.7 Prototype Hardware for 16 element array Digital Beam Former.

This modular design approach can also be used for ASIC design in the later stage of the development. The main features of the prototype developed are:

- FPGA – Virtex 5 FX130T
- Clock Domains
- Onboard Clock Oscillators : 32 MHz
- Clock distribution for ADC, DAC and DDS using CDCE62005 (Texas Instruments) with external clock input on SMA.
- 156.25 MHz clock oscillator for SFP
- 150 MHz clock oscillator for SATA interface
- Memory

- 2 GB DDR2 – SDRAM using MT16HTF25664H-667B
- 256Mb Flash Memory – JS28F256P30T95 from Numonyx
- 128 Mb SDRAM Memories - MT48LC4M32B2 from Micron
- Rocket IO interface @ 3.125 Gb/s
- Six SFP connectors are provided for SFP modules
- Analog Input
- Four, Two channel using, 16 bit, 125 MSPS ADC: AD9268 from Analog Devices
- Analog Output
 - One, Two channels using, 14 bit, 125MSPS DAC: DAC2904 from Texas Instrument
 - Eight , single channel, DDS : AD9954 from Analog Devices
- External Interfaces: Ethernet, USB 2.0 High Speed, Two RS-232 channel using MAX3223 on DB9, LVDS Interface.

V. RESULTS

The Fig. 8 shows the simulation results of the digital down converter and the complex multiplication of the weights to form multiple digital beams.



Fig. 8 Simulation of Digital Down Converter and multiple beams.

The developed multiple digital beam architecture is configured on the VIRTEX-V Field Programmable Gate Array (FPGA) and the results are captured on the chip-scope. The beams f ormed in real time are shown in Fig.9.

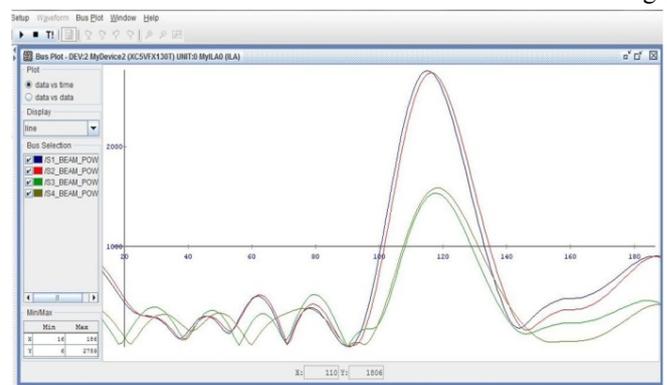


Fig. 9 Real time Beam captured from the chip-scope on the VIRTEX-V FPGA.

The real time data captured on the chip-scope is imported through USB interface to PC and plotted using the MATLAB.

The multiple beams have been plotted using the real time data as shown in Fig 9 for a resolution of 50.

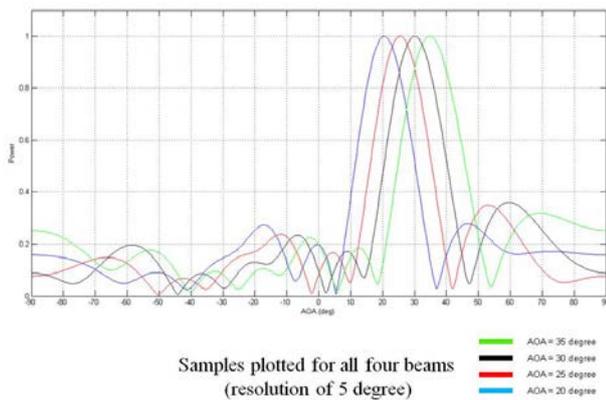


Fig. 9 Multiple Digital Beams in MATLAB plotted using Real time data captured from VIRTEX-V FPGA.

The virtex-V FPGA resources for this architecture to form a typical four beams are shown in below table.

Slice Logic Utilization	Used/Available	Utilization Ratio
Slice Registers	15705/81920	19%
Slice LUTs	10525/81920	12%
DSP Slices	306/320	95%
Block RAM Memory	69/298	24%

VI. CONCLUSION AND FUTURE SCOPE

We have developed a 4/8/16-element phased array multiple DBF system. The weights are calculated using the most efficient RLS algorithm. The Virtex-V FPGA is used for the spatial digital processing, and it has enabled a remarkable reduction in the area utilization compared to the discrete and analog versions. This pipelined architecture generates multiple beams up to maximum of 4 beams simultaneously from a given array matrix of 4/8/16 elements. Conventional methods of implementation of beam forming make the system cumbersome and sensitive to temperature and other unavoidable environmental conditions. FPGA based

implementation finds huge applications in modern radars as this implementation makes the system immune to the limitations that the analog methods face. At the same time, the proposed beam-forming system enjoys advantages of a reconfigurable design and low cost. DBFs have advantages such as fast adaptive null forming, the generation of several simultaneous beams, array self-calibration etc.

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