

Design and implementation of a high precision time synchronization method for borehole-surface microseismic monitoring

Yadongyang Zhu¹, Wenhao Wei^{2*}

¹School of Information Engineering, Beijing Institute of Petrochemical Technology, Beijing 102617, China

²North Automatic Control Technique Research Institute, Taiyuan 030006, China

Received: August 19, 2021. Revised: February 2, 2022. Accepted: February 15, 2022. Published: March 10, 2022.

Abstract—Borehole-surface monitoring can effectively improve the accuracy of the microseismic event location. It is necessary to strictly synchronize the acquisition time of borehole and surface monitoring nodes. However, the synchronization signal transmission through the logging cable will cause a delay. In this paper, a calibration method designed to compensate for the deviation of time synchronization due to long-distance transmission on the logging cable. First, the transmission delay of the pulse per second (PPS) is measured in the delay measurement stage. The delay from the global positioning system (GPS) module to all monitoring nodes can get in sequence. Second, in the delay compensation stage, each monitoring node is delayed for a particular time to ensure that all nodes start working simultaneously. Finally, a high-precision clock source is designed to drive the analog-to-digital converter (ADC) to avoid the crystal oscillator's accumulated error. To verify the accuracy of the calibration method, the modules were tested separately. The length of the logging cable used is 3000 meters. Through experimental verification, the method in this paper can be used to accurately control the time synchronization of different monitoring nodes in the borehole and on the surface within 1 μ s.

Keywords—Borehole-surface monitoring, Time synchronization, High-precision clock source, Pulse compensation.

I. INTRODUCTION

MICROSEISMIC monitoring is a commonly used method for hydraulic fracturing [1], [2]. It is an indispensable and essential technical means for shale gas exploration [3] and an enhanced geothermal system [4]. Using the technique of borehole-surface microseismic monitoring, a good monitoring perspective is obtained in both the horizontal and vertical directions [5], [6]. Compared with traditional monitoring

methods, it can effectively improve the positioning accuracy of microseismic events. The factors that affect the accuracy of microseismic monitoring are closely related to the first arrival picking. Therefore, it is necessary to strictly synchronize the monitoring data in the borehole with the monitoring data on the surface. The monitoring system on the surface can use GPS for time synchronization [7]. When GPS is used to synchronize the monitoring system in the borehole, the transmission of the signal through the logging cable will cause a delay, which will cause an error between the acquisition time of the borehole system and the surface system.

A standard method uses a phase-locked loop (PLL) to synchronize the clocks between different acquisition nodes [8]. Another approach is to use network synchronization, such as the IEEE1588 protocol [9]. However, there are restrictions when the above techniques apply to the monitoring systems in the borehole. Firstly, the PLL is suitable for environments with short transmission distances, not ideal for long cables. The IEEE1588 protocol is based on the network, and the network communication protocols will waste transmission bandwidth for cable communication [10]. Secondly, the monitoring system in the borehole is under a high-temperature and high-pressure environment, which will significantly impact the accuracy of the crystal oscillator [11]-[13].

In this paper, a calibration method is designed to compensate for time synchronization's deviation due to long-distance transmission on the logging cable. Meanwhile, a crystal oscillator compensation method is designed so that the ADC can still maintain the stability and accuracy of data acquisition when it works for a long time.

II. THE SYNCHRONIZATION SCHEME

The block diagram of the time synchronization method used in the borehole monitoring system shows in Figure 1. The surface part comprises a GPS module and measurement module based on a field-programmable gate array (FPGA). The borehole part includes a delay compensation module and clock

module based on an FPGA.

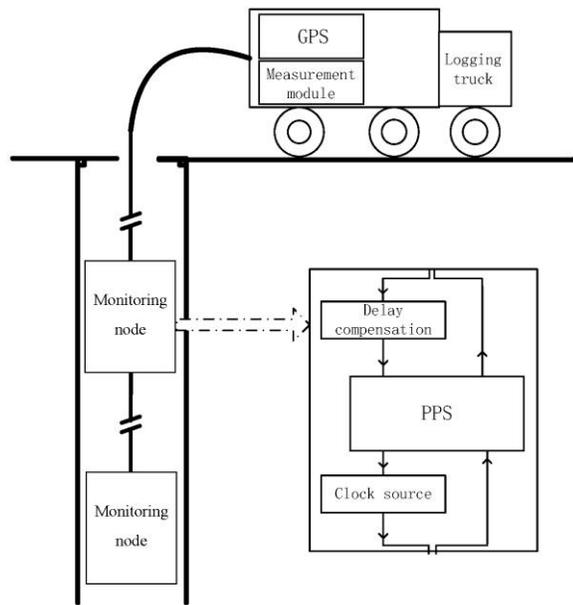


Fig. 1 the time synchronization method used in the borehole system

In the delay measurement stage, the transmission delay of the PPS is measured. The delay measurement method is that the system sends a simulated PPS. When the monitoring node receives the simulated PPS, it returns the signal to the surface module. Then half of the difference between the sending time and the receiving time is the delay from the GPS module to the monitoring node. The delay from the GPS module to all monitoring nodes can be measured in sequence. In order to ensure measurement accuracy, a method of taking multiple measurements and averaging can be used.

In the delay compensation stage, according to the value measured by the delay measurement module, each monitoring node is delayed for a particular time to ensure that all nodes start working simultaneously.

The purpose of the above modules is to ensure the ADC in the motoring nodes starts working simultaneously. Meanwhile, A crystal oscillator generates the sampling clock of ADC. Long-term operation of the crystal oscillator will cause accumulated errors. Two adjacent PPS can measure the number of pulses generated by the crystal oscillator. Disperse the error of the crystal oscillator in multiple cycles within 1s for compensation to eliminate the influence of the accumulated error of the crystal oscillator on the ADC.

III. THE SYNCHRONIZATION SCHEME

A. Delay measurement module

During the delay measurement, the FPGA on the surface generates a simulated PPS. Simultaneously, FPGA starts counting with the pulses generated by the temperature-compensated crystal oscillator. The simulated PPS is transmitted to the monitoring nodes in the borehole through the

logging cable. When the monitoring node receives the simulated PPS, it returns the signal to the surface module. The Block diagram of the delay measurement module is shown in Figure 2.

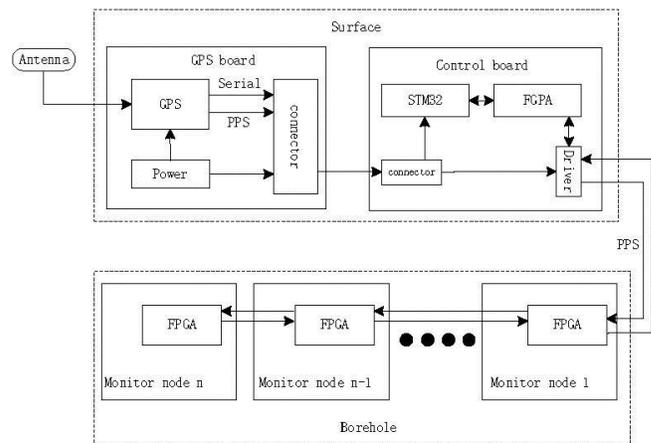


Fig. 2 block diagram of the delay measurement module

This stage completes the following functions:

(1) The delay measurement module in FPGA on the surface generates a simulated PPS and transmits it to each monitoring node through the logging cable.

(2) FPGA measures the time from the delay measurement module to the monitoring nodes.

(3) Calculate the delay from FPGA to each monitoring node.

(4) Store the delay in the memory of each monitoring node.

A counter clocked by a 100MHz temperature-compensated crystal oscillator uses on the surface. The delay measurement module starts timing and sends the simulated PPS Simultaneously. The first monitoring node receives the PPS, sends it back to the surface. When the delay measurement module detects the returned signal, it stops timing and gets the value. The delay from each monitoring node to the surface FPGA measures is analogous.

The value obtained by the delay measurement module can transmit to each monitoring node for subsequent processing. In general, the usage model of the borehole instrument is fixed. Thus, after getting the delay, it can store each monitoring node's internal memory.

B. Delay compensation module

Effective compensation methods must take after obtaining the PPS transmission delay in the logging cable. The delay of the GPS module to each monitoring node is different. When monitoring nodes receive the PPS, they can delay for a particular time so that the ADC starts synchronously. The delay compensation method shows in figure 3.

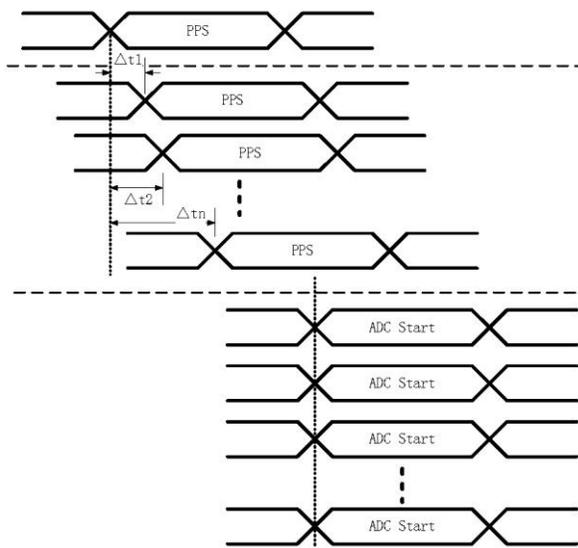


Fig. 3 the delay compensation method

The monitoring node in the borehole uses a high-temperature resistant crystal oscillator and has an extensive working temperature span due to the different external environments. As time increases, the output of the crystal oscillator is uncertain. In the case of constant temperature, the output of the crystal oscillator can remain stable in a short time. The interval time between two adjacent PPS generated by the GPS module is fixed. It can use to count the output of the crystal oscillator.

The sampling rate commonly used in seismic monitoring is generally 250Hz, 500Hz, 1000Hz, 2000Hz, and 4000Hz. Take a 3000m cable as an example. The PPS transmission delay in the logging cable should be about 20μs. To ensure the integrity of the monitoring data and convenience to store, align the start working time of monitoring nodes in seconds. The crystal oscillator can generate a delay of 999980μs, ensuring the starting time of the ADC. The delay compensation module comprises three parts: counter unit, delay setting unit, and compensation unit, as shown in Figure 4.

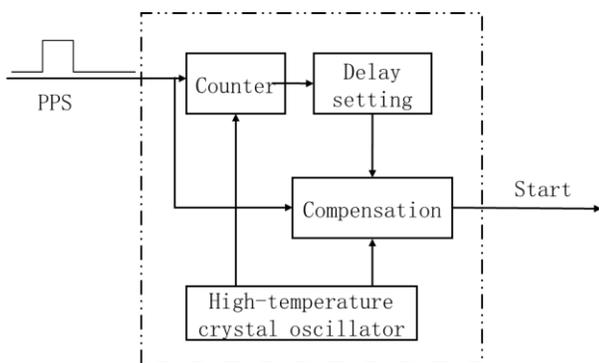


Fig. 4 block diagram of the delay compensation module

The module mainly completes the following functions:

(1) The PPS enables the counter unit and counts the pulses generated by the crystal oscillator. After receiving the PPS twice, the counter unit completes counting and transmits the value to the delay setting unit.

(2) The delay setting unit determines the number of pulses that need to compensate and whether to add or delete pulses. Then, the delay setting value transmits to the compensation unit.

(3) The compensation unit receives the delay setting value and enables the unit. When a new PPS arrives, it starts counting. A pulse sends when the count completes allowing the ADC to start the acquisition.

The crystal oscillator frequency used is 100MHz, the error is 70ppm. The frequency counting range is 99993000~100007000. When the transmission delay is $t_{delay}=20\mu s$, it is necessary to delay $t_D=999980\mu s$ to make up a sampling period, use the crystal oscillator with frequency $f=100MHz$ to count 99998000 times. When there is an error in the output of the crystal oscillator, the accurate value, upper limit, and lower limit of the frequency are, respectively $count=100000000$, $count_{up}=100007000$, $count_{down}=9993000$. Then the count value required can obtain according to the formula:

$$x/count_d = count_{up/down} / count \quad (1)$$

Then calculated the upper limit and lower limit of x are $x_{up} = 100004999.86$, $x_{down} = 99991000.14$. That is to say, the difference between the count value and the actual value is at most one crystal oscillator cycle, which is 10ns.

C. High precision clock reference source

The delay measurement and compensation aim to ensure the ADC in motoring nodes starts working simultaneously. The ADC used in the borehole is ADS1282, which requires an external crystal oscillator with a frequency of 4.096MHz. In this paper, a high-precision clock source is designed to drive the ADC to avoid the accumulated error of the crystal oscillator.

The clock source uses the fundamental clock frequency of an 8.192MHz high-temperature crystal oscillator. The clock source is composed of a crystal oscillator, PPS receiving module, and clock compensation module. The structure shows in Figure 5. The purpose of using an 8.192MHz crystal oscillator is to facilitate the compensation of the fundamental clock frequency of 4.096MHz. When the fundamental clock frequency is less than 4.096MHz, the 8.192MHz pulse signal can insert.

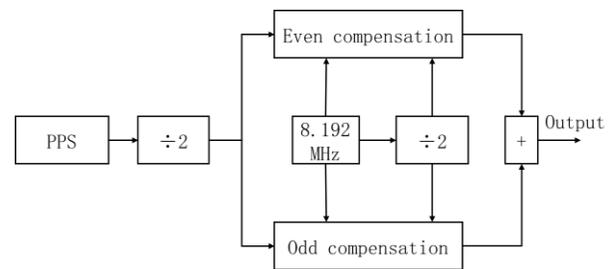


Fig. 5 the structure of clock source

The PPS receiving module divides the PPS by two and outputs it to obtain a 0.5Hz square signal. The purpose of dividing is to separate the fundamental clock signal into two groups for compensation. After counting the crystal oscillator in 1st-second, it takes a particular time to compensate, which will cause the next second to be inaccurate. Therefore, the crystal

oscillator output is divided into odd and even groups, leaving enough processing time for compensation.

The 0.5Hz square signal uses as a control, the odd-numbered second $(2n+1)$ counter enables at a high level, and the even-numbered second $(2n+2)$ counter enables at a low level. Determine how to compensate the clock source according to the counter and the theoretical value difference. If the difference is negative, pulse needs to add, and if the difference is positive, pulse needs to delete.

The fundamental clock frequency is 4.096MHz, and the accuracy is 70ppm, so the maximum number of errors counted in one second is 280. The pulse compensation should be equally divided within 1s. This article divides the 4.096MHz oscillation into 512 groups. The number of compensation pulses n should be distributed in the first n groups of 512.

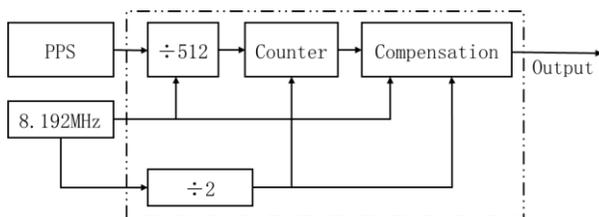


Fig. 6 block diagram of clock source for group compensation

The Block diagram of the clock source for group compensation is as shown in Figure 6. The 8.192MHz crystal oscillator is divided by 2 to obtain 4.096MHz as the fundamental clock. The output of the crystal oscillator is frequency-divided to generate a 512Hz signal. If the compensation difference is negative, replace the current pulse with an 8.192MHz pulse. Figure 7 shows the compensation for this situation. If it is positive, set the output low. Figure 8 shows the compensation for this situation.

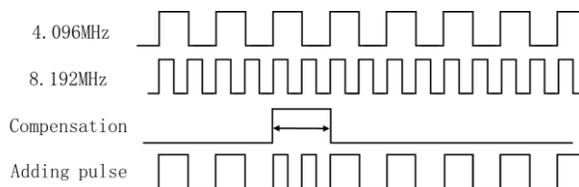


Fig. 7 the principle of compensation for adding pulses

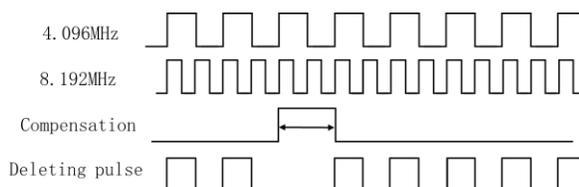


Fig. 8 the principle of compensation for deleting pulses

When starting to count, there is uncertainty in the clock phase at the starting time. Therefore, it is necessary to include a fundamental clock of 8.192MHz with a clock period of 125ns while calculating the error.

IV. EXPERIMENTAL RESULTS AND ANALYSIS

The time synchronization system in consists of a surface module and borehole module. The surface module sends the PPS to the monitoring node in the borehole. It is composed of a GPS board and an FPGA board. Figure 9(a) shows the GPS board. Figure 9(b) shows the FPGA board. The GPS board communicates with the computer through the network and controls the FPGA board to send PPS. The FPGA board in the monitoring node is responsible for delay compensation and clock reference source, as shown in Figure 9(c).



(a) GPS board



(b) FPGA board



(c) the monitoring node's FPGA board

Fig. 9 the composition of the time synchronization system

To verify the accuracy of the synchronization system, the above modules were tested separately. The length of the logging cable used for the test is 3000 meters. The measuring equipment is a Tektronix MDO4054C oscilloscope with a bandwidth of 500MHz and a sampling rate of 2.5GS/s. In the test, use it to capture and display the waveform.

A. Delay measurement test

This section tests the delay caused by the transmission of PPS. Channel 1 of the oscilloscope measures the pulse signal output from the logging cable, and Channel 2 measures the pulse signal input to the logging cable.

Figure 10 shows the PPS send at the surface module with a 10% duty cycle. Figure 11 is the PPS measured at the surface module and borehole module. Figure 12 compares the rising edges of the two waveforms from Figure 11. It can find that the transmission of the PPS through a 3000m cable produces a delay of about 18.6 us.

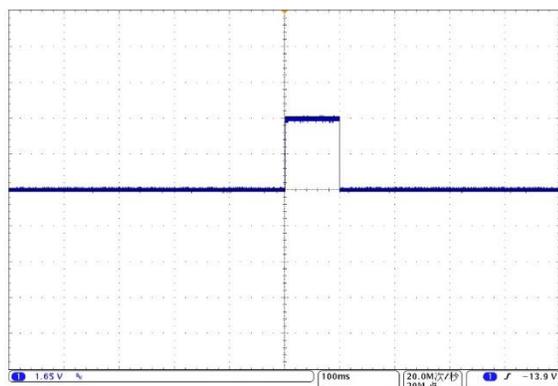


Fig. 10 a simulated PPS

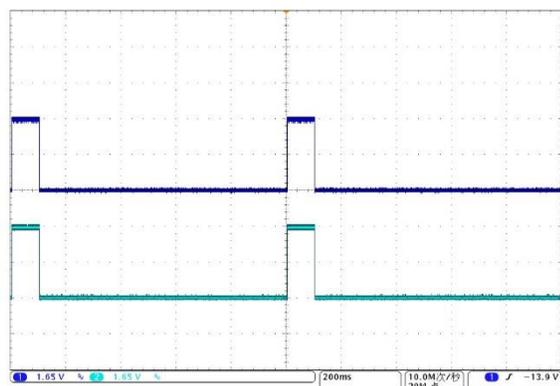


Fig. 11 PPS at the transmitter and receiver

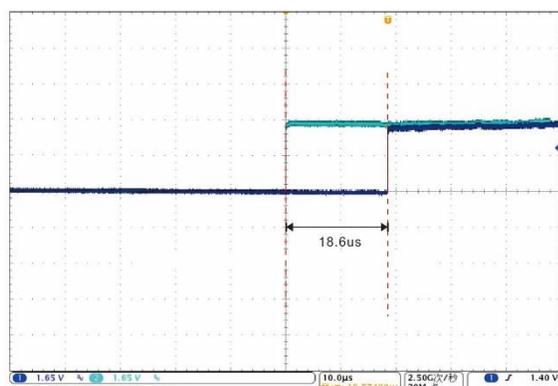


Fig. 12 delay caused by PPS transmission via cable

B. Delay compensation test

This section compares the difference between the compensated pulse and the PPS generated by the GPS. Channel 1 of the oscilloscope measures the compensated pulse, and channel 2 measures the PPS, the comparison results shown in Figure 13. It can find from the rising edge comparison in Figure 14, and the difference is 38.4ns.

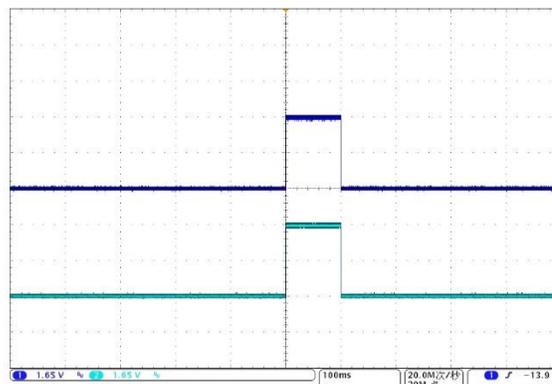


Fig. 13 waveform comparison of PPS

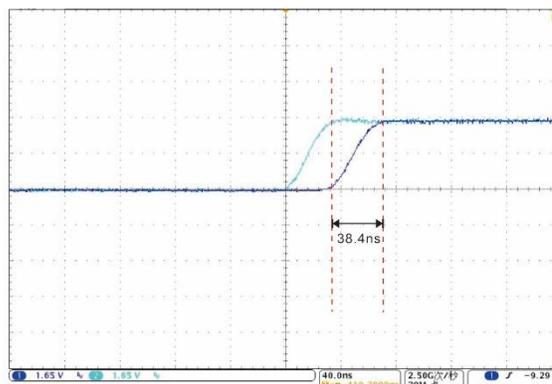


Fig. 14 waveform comparison of PPS rising edge

Five tests were carried out to verify the stability of the delay compensation module. The interval between each test ranged from 1 to 2 days. Ten measurements were taken for each test. The measurement results show in Table 1. The table's average value of the measurement data is 50.7ns, and the mean square error is 8.6ns.

Table 1 the measurement results (ns)

No.	Test1	Test 2	Test 3	Test 4	Test 5
1	38.4	53.3	64.1	36.6	59.3
2	36.1	56.0	55.3	64.9	50.2
3	61.3	45.5	62.9	62.2	46.3
4	56.4	48.8	48.9	51.3	48.2
5	45.6	60.1	60.9	51.1	47.9
6	55.8	60.5	64.7	48.6	48.8
7	36.6	48.2	44.5	62.1	64.4
8	43.5	49.1	36.9	60.5	58.9
9	53.0	52.1	48.4	52.5	52.6
10	39.1	53.3	36.3	37.0	40.9

C. Clock reference source test

This section measures the compensation of the clock source. The Chipscope logic analyzer component of the ISE software uses to measure the compensated clock. The output of the crystal oscillator triples by FPGA and operates as the sampling clock of the logic analyzer to measure the clock source. Figure 15 is the waveform of the adding pulse, and Figure 16 is the waveform of the deleting pulse.

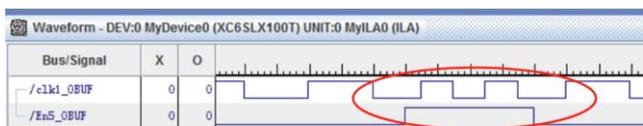


Fig. 15 the waveform of the adding pulse

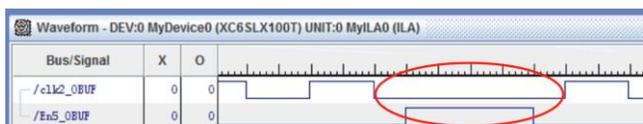


Figure 16 the waveform of the deleting pulse

We compare the monitoring data from the borehole and surface to verify the validity of the clock source under long-term operation. The borehole and surface nodes are placed in the same environment and generate seismic waves by hitting the ground.

The first step is to use an uncompensated clock source for data acquisition. After a few hours of regular work, we conducted a data test. Figure 17 shows the waveforms acquired from the same hitting event by borehole and surface nodes. Figure 18 selects 200 consecutive sampling points for comparison. The number of sampling points has begun to deviate through contrast, about 4 to 5 sampling points.

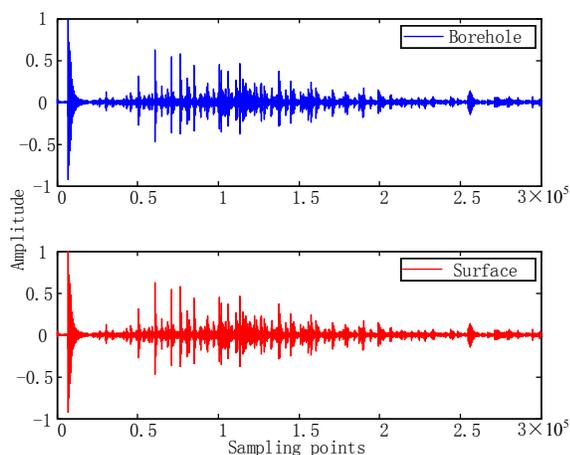


Figure 17 comparison of monitoring data with an uncompensated clock source

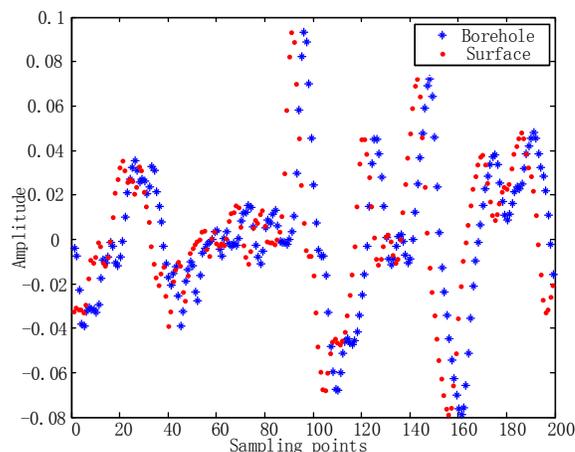


Figure 18 select 200 points to compare an uncompensated clock source

The second step is to use a compensated clock source for data acquisition. Similarly, after a few hours of regular work, we conducted a data test. Figure 19 shows the waveforms acquired from the same hitting event by borehole and surface nodes. Figure 20 selects 200 consecutive sampling points for comparison. Through comparison, it can find that the sampling points are very close, and the sampling time interval between the two sampling points is close to 400ns.

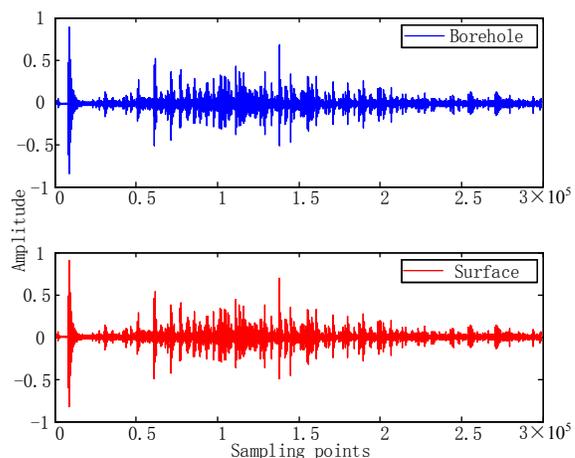


Figure 19 comparison of monitoring data an compensated clock source

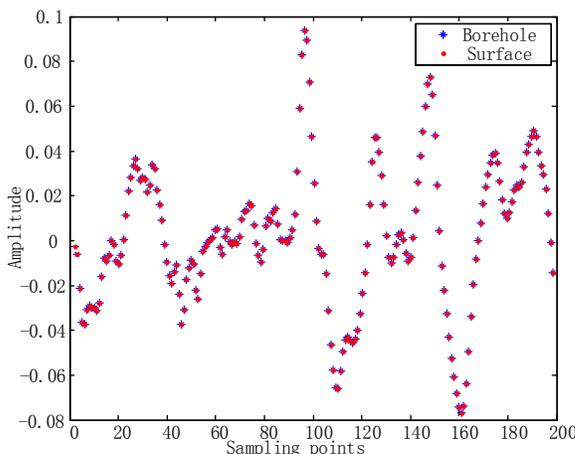


Figure 20 select 200 points to compare an compensated clock source

V. CONCLUSION

This paper focuses on the synchronization signal delay caused by the cable transmission. The temperature-compensated crystal oscillator is used on the surface to measure the delay, and the high-temperature crystal oscillator is used in the borehole to compensate. Aiming at the high-temperature crystal oscillator's accumulated error in the borehole, compensation methods propose the delay compensation module and the ADC clock source, respectively. The method in this paper can ensure that the error between the initial sampling point of the ADC in the borehole and surface is less than 100ns. To compensation the ADC clock source, we use PPS to count the crystal pulses at a fixed time interval and decide whether to insert or delete pulses. The pulse compensation divides into multiple periods of 1s. This method can control the synchronization error of the ADC within 400ns. The experiment results show that the proposed method can strictly synchronize the monitoring data in the borehole with the monitoring data on the surface. We will build a deep learning model on the crystal oscillator's offset compensation to suppress the accumulated error in future work.

ACKNOWLEDGMENT

This work was supported by the Natural Science Foundation of China (grant no. 42104175); General Project of Science and Technology Plan of Beijing Municipal Education Commission (grant no. KM202010017011).

References

- [1] J. P. Vermynen, M. D. Zoback. Hydraulic Fracturing, Microseismic Magnitudes, and Stress Evolution in the Barnett Shale, Texas, USA[C]. *SPE Hydraulic Fracturing Technology Conference*, 2011, SPE-140507-MS,
- [2] N. Li, L. Fang, W. Sun, et al. Evaluation of Borehole Hydraulic Fracturing in Coal Seam Using the Microseismic Monitoring Method[J]. *Rock Mechanics and Rock Engineering*, 2021, 54(2): 607-625.
- [3] W. Sun, L. Fu, X. Guan, et al. A study on anisotropy of shale using seismic forward modeling in shale gas exploration[J]. *Chinese Journal of Geophysics*, 2013, 56(3): 961-970.
- [4] J. Folesky, J. Kummerow, S. A. Shapiro, et al. Rupture directivity of fluid - induced microseismic events: Observations from an enhanced geothermal system[J]. *Journal of Geophysical Research: Solid Earth*, 2016, 121(11): 8034-8047.
- [5] Y. D. Y. Zhu, N. Li, F. Sun, et al. Design and application of a borehole-surface microseismic monitoring system[J]. *Instrumentation Science & Technology*, 2017, 45(3): 233-247.
- [6] Y. D. Y. Zhu, J. L. Wang, F. Sun, et al. Micro-seismic monitoring and instrument for hydraulic fracturing in the

low-permeability oilfield[J]. *Chinese Journal of Geophysics*, 2017, 60(11): 4282-4293.

[7] D. Pallier, V. Le Cam, S. Pillement. Energy-efficient GPS synchronization for wireless nodes[J]. *IEEE Sensors Journal*, 2020, 21(4): 5221-5229.

[8] V. Ostrouhov, M. Korzhavin, M. Grigor'ev. Synchronization System for Semiconductor Frequency Converters with a Power Supply Network[J]. *Russian Electrical Engineering*, 2020, 91(5): 316-320.

[9] T. Cooklev, J. C. Eidson, A. Pakdaman. An implementation of IEEE 1588 over IEEE 802.11 b for synchronization of wireless local area network nodes[J]. *IEEE Transactions on Instrumentation and Measurement*, 2007, 56(5): 1632-1639.

[10] J. Han, D. Jeong. A practical implementation of IEEE 1588-2008 transparent clock for distributed measurement and control systems[J]. *IEEE Transactions on Instrumentation and Measurement*, 2009, 59(2): 433-439.

[11] Y. Roh, A. Asiz, W. Zhang, et al. Experimental study and theoretical prediction of aging induced frequency shift of crystal resonators and oscillators[J]. *Microelectronics Reliability*, 2003, 43(12): 1993-2000.

[12] R. Karlquist, L. Cutler, E. Ingman, et al. A low-profile high-performance crystal oscillator for timekeeping applications[C]. *Proceedings of International Frequency Control Symposium*, 1997, IEEE, 873-884.

[13] O. Baran, M. Kasal. Study of oscillators frequency stability in satellite communication links[C]. *2009 4th International Conference on Recent Advances in Space Technologies*, 2009, IEEE, 535-540.



Yadongyang Zhu, male, was born in March 1987. His title is assistant professor. In 2010, he received a bachelor's degree in instrument science and technology from Jilin University. In 2018, he received a Ph.D degree in instrument science and technology from Jilin University. He is now working in the Beijing Institute of Petrochemical Technology. His research fields include geophysical instruments and IoT. He has published 5 papers and participated in 4 scientific research projects.



Wenhao Wei, male, was born in November 1987. His title is senior engineer. In 2010, he received a bachelor's degree in instrument science and technology from Jilin University. In 2013, he received a master's degree in instrument science and technology from Jilin University. He is now working at North Automatic Control Technology Research Institute. His research field is embedded systems. He has published 2 papers and participated in 6 scientific research projects.

Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

Yadongyang Zhu proposed a calibration method to compensate for the deviation of time synchronization due to long-distance transmission on the logging cable. Yadongyang Zhu and Wenhao Wei conducted the experiments and analyzed the results. All authors discussed the results and wrote the manuscript.

Creative Commons Attribution License 4.0 (Attribution 4.0 International, CC BY 4.0)

This article is published under the terms of the Creative Commons Attribution License 4.0

https://creativecommons.org/licenses/by/4.0/deed.en_US